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Defect Analysis and Testing of Low Power Nanoscale Reversible Decoder using Quantum Dot Cellular Automata

R. Jayalakshmi[1,*], M. Senthil Kumaran[2]

[1]*ECE Department, Sri Chandrasekharendra Saraswathi Viswa Maha Vidyalaya, Enathur – 631 561, Tamil Nadu, India.*
[2]*CSE Department, Sri Chandrasekharendra Saraswathi Viswa Maha Vidyalaya, Enathur – 631 561, Tamil Nadu, India.*

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ABSTRACT

The present research focusses on analysis of defects and the framework for testing the reversible decoder constructed using quantum dot cellular automata circuits. Quantum dot cellular automata has been one of the paradigms shifts from the conventional complementary metal oxide field effect transistor. This paper focuses on the modeling of struck at faults that possibly occurs in a circuit other than the fabrication defects. The struck at faults are modeled considering the inverter and the majority voter. We have also created a model for the flow of signal on the reversible decoder using quantum dot cellular automata. The design analyses the percentage of fault occurrence for the decoder constructed using reversible QCA2 Gate. The model is simulated using QCA Designer tool.

1. Introduction

The scaling of the Complementary metal oxide semiconductor field effect transistor has reached the threshold leading to the quantum mechanical effects in the sub-atomic scale as Per Moore's law [1]. Qubit is the fundamental unit used in quantum computing and the quantum gates are reversible in nature, due to which the energy dissipation is ideally zero [2, 3]. The reversible quantum gates can be constructed using quantum dot cellular automata, which uses charge confinement protocol. The design can be analyzed for the defects and the tolerance towards fault and the occurrence of the error in the output can be predicted by performing Fault analysis on the circuit under design [4-6]. In this work, the reversible decoder constructed using QCA2 gate is analyzed for Struck at faults and the error analysis is performed. Further the design has been tested for its energy dissipation for the changes in the temperature.

1.1 Background of QCA

The quantum dot cellular automata (QCA) consists of a cell in which four quantum wells are fabricated for the electrons to occupy the antipodal sites to represent the values of 0 and 1 through the polarization of -1 and +1, [7, 8] as represented in Fig. 1. The other configurations of quantum dot cellular automata includes a QCA wire, inverter and majority voter [8-10] as in Figs. 2 and 3. The majority voter of a QCA can be used to function as a AND gate or and OR gate by fixing the polarity of one of the inputs to +1 or -1 [8-10] represented in Fig. 4. The data is transmitted using Clocking mechanism which consists of four phases of clock cycles like switch, hold, release and relax [10]. There are two types of cross overs namely coplanar and multilayer cross over [7-10].

Fig. 1 QCA Cell with P = -1 and P = +1

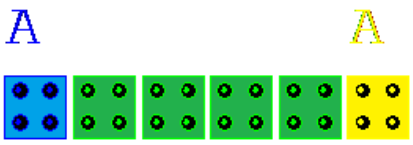

Fig. 2 QCA Wire

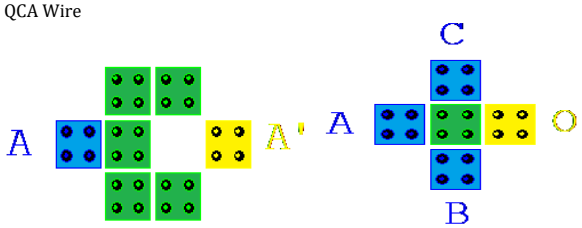

Fig. 3 Inverter and three input majority voter configurations

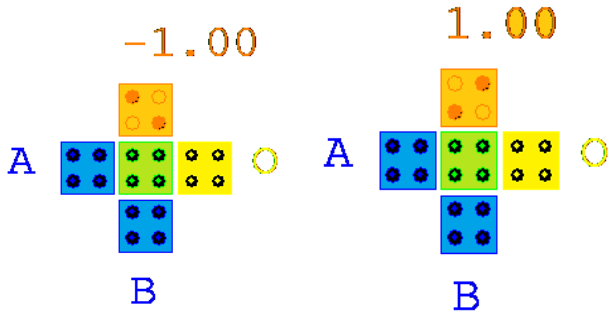

Fig. 4 AND and OR gate implementation using three input majority voter configurations

2. Existing Design of Reversible Decoder

As designed by Jayalakshmi et al. [3], a reversible decoder is constructed by utilizing the QCA2 gate with the input vectors A, B, C corresponding to the output vectors P, Q, R. As designed by Jadav das et al. [2], the 1-to-2 decoder is constructed by fixing the input A to the logic '0' as in Fig. 5. The input B is fixed at E_n and C input at W_0 as represented in the Fig. 6 with the output leading to $Y_1 = E_nW_0$ and $Y_0 = E_nW_0'$ with the out R being neglected as garbage output [3]. The simulations are performed using QCA Designer tool developed by the Walus lab [11].

*Corresponding Author:jayalakshmiecescsvmv@gmail.com(R. Jayalakshmi)

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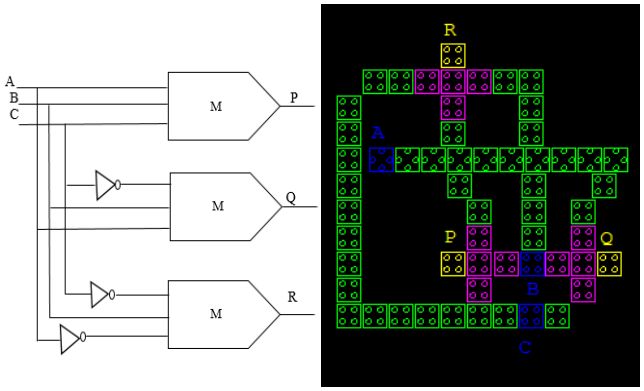


Fig. 5 QCA schematic of QCA2 gate and QCA layout of QCA2 gate

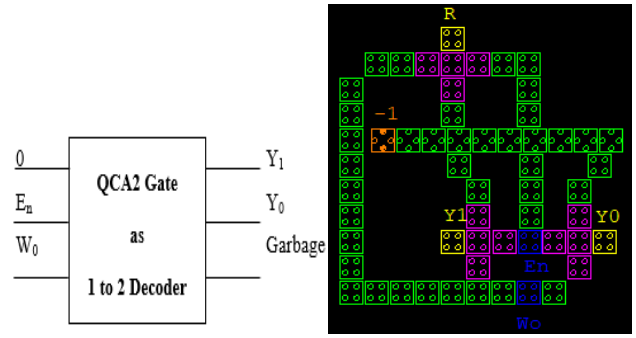
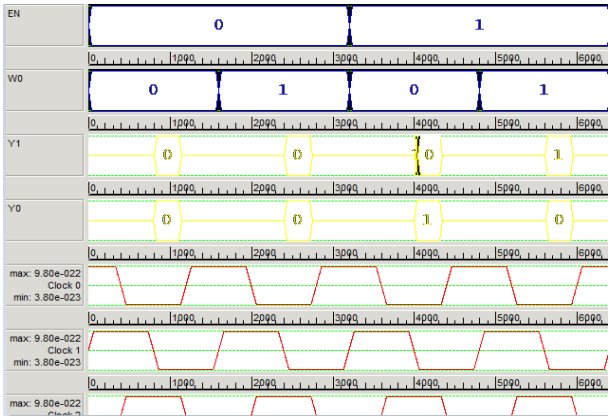


Fig. 6 Block diagram and layout of QCA2 gate as 1 to 2 decoder



E_n	W_0	Y_1	Y_0
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

Fig. 7 Simulation output and truth table of QCA2 gate as 1 to 2 decoder

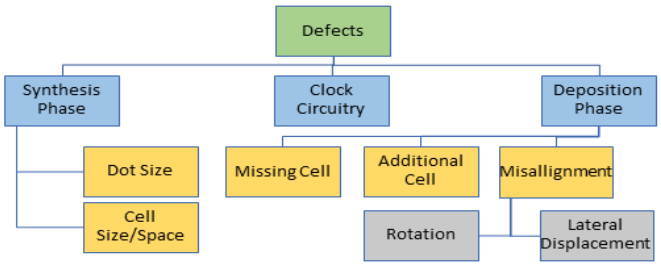


Fig. 8 Classification of defect in QCA circuits

3. Types of Defects

In a quantum dot cellular automaton circuits, the possible defects occur at the synthesis phase and deposition phase depending on metallic QCA and molecular QCA. Since clocking performs a crucial purpose the defects are fabricated due to the clocking circuitry as given in Fig. 8. In synthesis phase during fabrication the defect can occur because of the dot size and the space in which it is deposited [12-15]. During the deposition phase, the possibility of defect is due to the Misalignment, or addition of an extra cell or due to the absence of the required cell [15-17]. Numerous simulations on defects and fault injection has been evaluated on the QCA structures like inverter, wire, majority voter, cross over and fan outs. The displacement and misalignment defects are discussed by various authors [12-15] and represented in Figs. 9 and10.

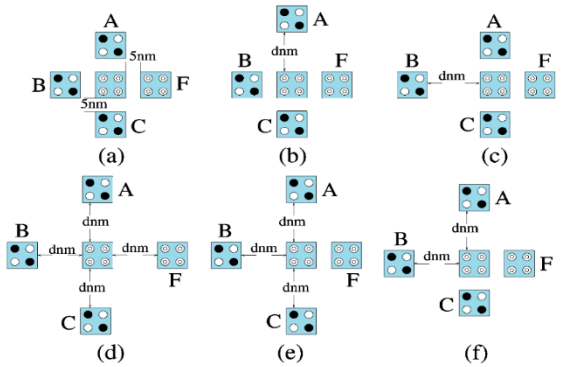


Fig. 9 Displacement in MV (a) fault free, (b) displace a, (c) displace b, (d) displace all inputs and output, (e) displace all inputs and (f) displace A and B

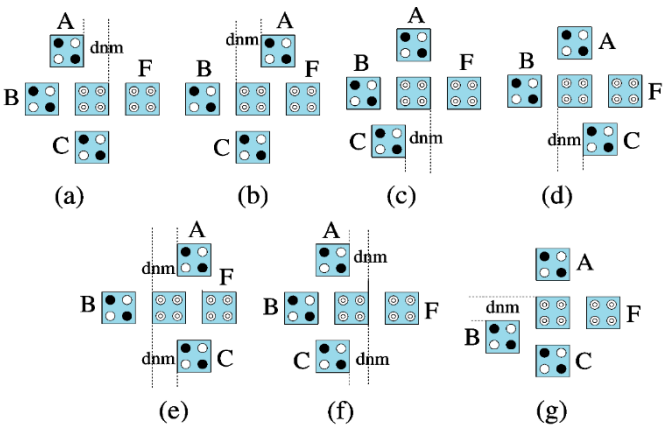


Fig. 10 Misalignment in MV (a) A misalignment, (b) A misalignment, (c) C misalignment, (d) C misalignment, (e) A, C misalignment, (f) A, C misalignment and (g) B misalignment

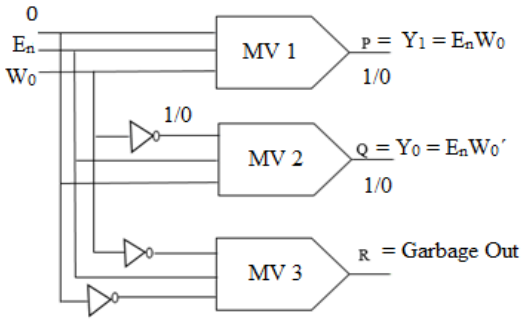


Fig. 11 Fault analysis of reversible decoder

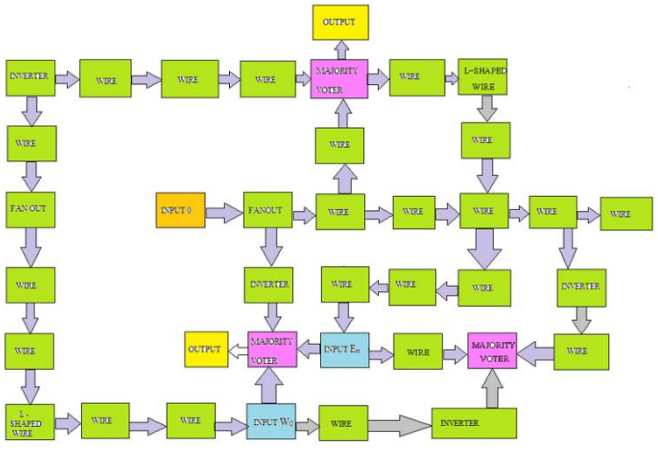


Fig. 12 Block diagram of reversible decoder circuit in QCA

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4. Defect Analysis of Reversible Decoder

Defect injection is crucial to study the behavior of QCA circuit under study and the Fault occurrence of the Majority Voter and Inverter are studied [12-18]. In this present work the defect characterization of the circuits is done at the logic level. The reversible decoder has three majority voters MV1, MV2 and MV3 which corresponds to the output P, Q and R as shown in Fig. 11. Since the output R is garbage the defect analysis is performed for the majority voters MV1 and MV2 and the inverter corresponding to the majority voter MV2. The effect of struck at fault is studied in which s-a-0 and s-a-1 are injected for the inputs E_n and W_0. In Fig. 12 the block diagram represents the reversible decoder interims of the different QCA configurations, where in the possibility of defects can occur. The work presented here is based on majority voter and inverter for defect analysis.

Table 1 Struck at fault analysis for different input conditions

Input		Fault free output		Mv1 faulty out (y_1)				Inverter Faulty out		Mv2 faulty out (y_0)			
E_n	W_0	Y_1	Y_0	E_n s-a-0	W_0 s-a-0	E_n s-a-1	W_0 s-a-1	s-a-0	s-a-1	E_n s-a-0	W_0 s-a-0	E_n s-a-1	W_0 s-a-1
0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	0	0	0	1	0	1	0	0	0	1	0
1	0	0	1	0	0	0	1	1	0	0	0	0	1
1	1	1	0	0	0	1	1	1	0	0	0	1	1

Table 2 Test vectors and fault conditions

(E_n, W_0)	(Y_1, Y_0)	(E_n, W_0)	(Y_1, Y_0)	(E_n, W_0)	(Y_1, Y_0)	(E_n, W_0)	(Y_1, Y_0)	(E_n, W_0)	(Y_1, Y_0)
(0,0)	(0,0)	(0,0)	(0,0)	(0,0)	(0,0)	(1,0)	(0,0)	(0,1)	(0,0)
(0,1)	(0,0)	(0,1)	(0,0)	(0,0)	(0,0)	(1,1)	(1,1)	(0,1)	(0,0)
(1,0)	(0,1)	(0,0)	(0,0)	(1,0)	(0,0)	(1,0)	(0,0)	(1,1)	(1,1)
(1,1)	(1,0)	(0,1)	(0,0)	(1,0)	(0,0)	(1,1)	(1,1)	(1,1)	(1,1)

Table 3 Error percentage for the test vectors

(Y_1, Y_0)/FF	(Y_1, Y_0)/F	(Y_1, Y_0)/F	(Y_1, Y_0) /F	(Y_1, Y_0) /F	Error%
(0,0)	(0,0)	(0,0)	(0,0)	(0,0)	0%
(0,0)	(0,0)	(0,0)	(1,1)	(0,0)	25%
(0,1)	(0,0)	(0,0)	(0,0)	(1,1)	25%
(1,0)	(0,0)	(0,0)	(1,1)	(1,1)	50%

Table 4 Temperature and energy dissipation analysis

Temperature (K)	Total energy dissipation (e-002 eV)	Average energy dissipation per cycle (e-003 eV)
1	3.34	3.04
2	3.30	3.00
3	3.18	2.89
4	3.09	2.81
5	3.04	2.76
10	2.47	2.25
15	2.29	2.08
20	2.05	1.87
30	1.68	1.53
40	1.50	1.36
50	1.35	1.23

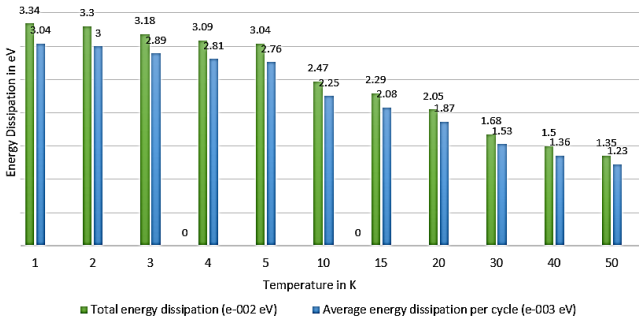

Fig. 13 Temperature and energy dissipation analysis

Table 1 represents the fault free outputs for the inputs E_n and W_0, along with the faulty output on injecting struck at fault for E_n and W_0 for both s-a-0 and s-a-1 , by calculating the output using $Y_1 = E_nW_0$ and $Y_0 = E_nW_0'$. In Table 2 the different test vectors along with the fault free and faulty vector outputs are given. In Table 3, the error percentage or the defect tolerance of the majority voters are given. The deviation from the fault free (FF) output to the faulty (F) outputs are obtained. The defect is maximum for the test vectors (1, 1), when struck at 1 occurs with a probability of occurrence of 0.25. The Table 4 represents the effect of temperature and energy dissipation, since the effect of temperature plays a major role in affecting the polarization of the output and can change the power dissipated throughout the transmission of signal. The power dissipation analysis is performed by using the QCA Designer E-tool [19]. The Fig. 13 plots the relationship between temperature and power dissipation which reflects the power dissipation is minimum at higher the temperature.

4. Conclusion

The research work focusses on the defect analysis performed on the Struck at faults on majority voter and inverter. The effect of the temperature and the energy dissipation is also studied. Since coplanar cross over is used, the configuration is more stable than the multilayer cross over structures. The reversible decoder structures can be used for higher order configurations and can be used to build the reversible configurable logic block for memory in quantum processor design.

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